REMARKS

Entry of this Amendment is proper because it narrows the issues on appeal and does not require further search by the Examiner.

Claims 1-20 are all the claims presently pending in the application. Claims 1, 2 and 20 have been amended to further define the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Applicant gratefully acknowledges that claims 14, 15, 17 and 18 would be allowed if rewritten in independent form. However, Applicant respectfully submits that all of the claims are allowable.

Claims 1-4, 8-13, 16 and 20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Hasegawa et al. (U.S. Patent No. 6,562,129). Claims 5-7 and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hasegawa.

These rejections are respectfully traversed in view of the following discussion.

I. APPLICANT'S INVENTION

The claimed invention (e.g., as recited in claim 1) is directed to a method of producing p-type Group III nitride compound semiconductor. The method includes forming a first Group III nitride compound semiconductor layer doped with p-type impurities, forming a second Group III nitride compound semiconductor layer **doped with substantially at least one of no impurities, n-type impurities, and n-type and p-type impurities**, such that an amount of impurities in said second Group III nitride compound semiconductor layer is less than an amount of impurities in said first Group III nitride compound semiconductor layer; and reducing a resistance of the first Group III nitride compound semiconductor layer one of after and during the forming of the second Group III nitride compound semiconductor layer.

Unlike conventional methods which form a p-type Group III nitride compound

semiconductor having a high electrical resistivity (e.g. higher than GaP or GaAs) (Application at page 3, lines 3-7), the claimed method forms (e.g., on the first Group III nitride compound semiconductor layer doped with p-type impurities) a second Group III nitride compound semiconductor **doped with substantially at least one of no impurities, n-type impurities, and n-type and p-type impurities**. This feature allows the resistance of the first Group III nitride compound semiconductor layer to be reduced (e.g., by performing a heat treatment).

II. THE HASEGAWA REFERENCE

The Examiner alleges that Hasegawa teaches the invention of claims 1-4, 8-13, 16 and 20 and makes obvious the invention of claims 5-7 and 19. Applicant would argue, however, that there are elements of the claimed invention that are not taught or suggested by the cited reference.

Hasegawa discloses a method in which a compound semiconductor layer including a p-type dopant is heated to allegedly eliminate atoms which deactivate the p-type dopant (Hasegawa at Abstract).

However, Applicant would submit that Hasegawa does not teach or suggest "*forming a second Group III nitride compound semiconductor layer doped with substantially at least one of no impurities, n-type impurities, and n-type and p-type impurities ...*", as recited, for example in claim 1 and similarly recited in claim 20. As noted above, this feature allows the resistance of the first Group III nitride compound semiconductor layer to be reduced (e.g., by performing a heat treatment).

Clearly, these features are not taught or suggested by Hasegawa. Indeed, Applicant would point out that a purpose of an exemplary aspect of the invention is to use a second Group III nitride compound semiconductor layer to reduce a resistance of a first Group III nitride compound semiconductor layer by moving some impurities in the first layer into the second layer. Hasegawa, on the other hand, merely teaches annealing a layer to reduce the resistance of the layer. That is, Hasegawa has nothing to do with moving impurities from a first layer to a second layer to reduce a resistance of the first layer.

In addition, the Examiner attempts to rely on Figure 8 and cols. 17 and 18 (e.g., embodiment 7) in Hasegawa to support his position. However, nowhere does this drawing

and these passages teach or suggest a layer "*doped with substantially at least one of no impurities, n-type impurities, and n-type and p-type impurities*" as in the claimed invention.

Specifically, the Examiner attempts to equate layer 36 in Hasegawa with the first Group III nitride compound semiconductor layer, and layer 37 with the second Group III nitride compound semiconductor layer. This is clearly unreasonable.

Indeed, Hasegawa teaches that layer 37 is a p-type cladding layer of p-type $Al_{0.07}Ga_{0.93}N$ with a dopant (magnesium) concentration of 5×10^{17} cm^{-3} (Hasegawa at col. 17, lines 14-22). That is, Hasegawa merely teaches that layer 37 may include p-type impurities. **Nowhere does Hasegawa teach or suggest that the layer 37 may include either 1) no impurities, or 2) n-type impurities, or 3) n-type and p-type impurities.** In fact, the Examiner concedes that none of the prior art teaches or suggests a second Group III nitride compound semiconductor layer having n-type impurities or n-type and p-type impurities on page 5 of the Office Action. Likewise, Hasegawa requires that layer 37 be p-type and thus, does not teach or suggest that the layer 37 may include no impurities.

The Application explains that the impurities (e.g., n-type, or n-type and p-type) in the second Group III nitride compound semiconductor layer (or lack of impurities) helps the p-type impurities existing in interstitial sites of the first Group III nitride compound semiconductor layer to be taken into the second Group III nitride compound semiconductor layer (Application at page 4, lines 18-25; page 9, line 24-page 12, line 7).

Nowhere is this taught or suggested by Hasegawa.

Therefore, Applicant would submit that Hasegawa does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

Applicant notes that a minor amendment has been made to claim 2 in order to address the Examiner's objection thereto.

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 8/24/05

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Tuan Nguyen, Group Art Unit # 2813 at fax number (571) 273-8300 this 24th day of August, 2005.

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